Remarks

Favorable action on the above-identified application in consideration of the above-made amendments and the following responsive remarks is respectfully requested.

Applicants note with appreciation the indication of allowability of independent claim 23.

With the above-made amendments, claims 1-27 and 30-31 remain pending in this application, of which independent claims 1, 2, 4, 15-17, 25, 26 and 30 as well as dependent claim 12 were amended. The independent claims were revised to further highlight the various characterizing aspects of the claimed invention including in a manner which clearly defines over the art documents, as applied in the outstanding rejections.

The set forth aspects directed to the mounting of the semiconductor device (e.g., semiconductor chip 1) are now further defined in each of the independent claims. For example, with regard to claim 1 and, similarly, in other ones of the independent claims, the set forth semiconductor device is now characterized as being both mounted on the principle side of the wiring substrate and electrically connected to the wiring of the wiring substrate via bump(s) of the semiconductor device. This can be seen with regard to the solder ball (bumps) 6 in Fig. 7, *et seq.*, of the drawings. Moreover, the previously existing expression "said principle side having a planar surface over its entirety" was also revised to unequivocally set forth that the entire principle side of the wiring substrate (e.g., module substrate 2 in Figs. 1, 2, 6, 7, etc.) has a common planar surface. Regarding the latter, although the previously existing language was intended to be interpreted as such, the changes presently being made should unequivocally avoid any question

of intent regarding this. Regarding dependent claim 12, the revision being implemented therein is strictly of a grammatical nature.

Previously pending dependent claim 25 was re-presented as an independent claim, incorporating the subject matter of the base independent claim 1 and was also revised to include the further clarification in which the entire principle side of the wiring substrate is a common planar surface (see example Fig. 19). That is, in view of the amendments being made to claim 1, regarding the mounting of the semiconductor device to the wiring substrate via bump(s) of the semiconductor device, it became necessary to re-present dependent claim 25 in a self-contained format so as to avoid conflict therewith. It is submitted, claim 25, as now amended, is also considered to be defining over the teachings of the applied art.

According to independent claim 1, the invention therein calls for a semiconductor module setting forth a wiring substrate, a semiconductor device, an external connection terminal and an insulating resin layer, in which the semiconductor device is mounted and electrically connected to wiring on the wiring substrate via bump(s) of the semiconductor device, and the entire said principle side of the wiring substrate being a common planar surface, as can be seen with regard to Figs. 1+, 6+, etc. The invention according to claim 1 further calls for the "external connection terminal" (e.g., 5) to be electrically connected to the wiring on the wiring substrate and also calls for an "insulating resin layer" (e.g., 10 or 10 and 30) which is provided between the wiring substrate and the external connection terminal and functioning as a stress relaxing layer between the semiconductor module and a board to which the module is mounted (see Figs. 16-19, 27-28, *et seq.*). Such featured aspects are also found with regard to other

ones of the independent claims, although they are presented in a somewhat modified form therefrom.

In independent claim 2, further, the set forth "insulating resin layer," which acts as a stress relaxing layer, has both an inclined portion and a flat portion, the flat portion being that on which the "external connection terminal" (e.g., 5) is arranged, and a part of the wiring electrically connected between a terminal (bump) on the semiconductor device and the external connection terminal of the module is formed on the inclined portion of the insulating resin layer. This can be seen in the example Fig. 1 of the drawings with regard to the wiring connections effected between the external connection terminals 5 on the flat surface of the insulating resin layer 10 (10 and 30) and the bumps 6 on the semiconductor device 1, the wirings including portions extending over the inclined portion of the insulating resin layer 10. Fig. 8F is an example showing regarding the formation of wires 3 over the inclined plane surface such as it relates to, for example, independent claim 4, and the shaping/patterning of the insulating resin layer which performs a stress relaxing function is implemented in a manner discussed in connection with Figs. 10A-10B, 12 and 35, in the Specification, the latter showing one example of the collective printing of the plural insulating layers on the wafer board, the wafer board including plural wiring substrates.

With regard to independent claims 15, 16 and 17, the invention therein sets forth a scheme in which the semiconductor device (e.g., including one or more chips) and the wiring substrate mutually are connected via bump(s) of the semiconductor device. As with regard to other claims, the module according to claim 15 features an insulating resin layer which acts as a stress relaxing layer and, further, calls for the wiring substrate to be a silicon substrate. This can be

seen with regard to Fig. 29 of the drawings, although not limited thereto, in which substrate 2 is a silicon substrate. Fig. 30, on the other hand, shows a like scheme which uses instead a glass substrate. In both claims 16 and 17, the invention therein calls for a connection to be effected between the semiconductor device (chip/chips) and the wiring substrate without the need of an underfill. With regard to independent claim 17, moreover, the invention calls for a "first insulating resin layer" which acts to relieve stress between the semiconductor module and the board to which the module is mounted as well as a "second insulating resin layer" which relieves stress between the chip and the wiring substrate.

Independent claims 26 and 30 also contain featured aspects covered by the above discussed independent claims, although in a somewhat modified form therefrom. With regard to independent claim 30, for example, the invention therein also calls for a stress relaxing layer between the semiconductor module and the board to which the module is mounted. This "insulating resin layer", according to claim 30, corresponds to one of plural such insulating resin layers that are collectively molded on the wafer board comprising a plurality of wiring substrates (see also independent claim 4). Further, each of the insulating resin layers is set forth as having a thickness greater than the semiconductor device between the wiring substrate and the external connection terminal. Related discussion of this is found, for example, beginning in paragraph [0208], on page 62 of the Substitute Specification. Additional related discussion is found from pages 20-24 of the Substitute Specification, regarding implementing the thickness of the stress relaxing layer and its relationship to the module itself.

The dependent claims also cover various details regarding the semiconductor module of the present invention. It is submitted, the invention

according to claims 1+, 2+, 4, 15, 16+, 17, 25, 26-27 and 30-31 could not have been attainable from the combined teachings of the references, as applied in the respective rejections.

Discussion will now turn to the respective rejections.

I. Rejection of Claims 1, 2, 5-8, 10-14, 24, 26, 27, 30 and 31 "insofar as definite," under 35 USC §103(a) over the combination of Launay (USP 6,320,753) in view of Yukawa (USP 6,436,733).

Each of the independent claims now call for the entire principle side of the wiring substrate (the side on which the semiconductor device is mounted) to be a common planar surface (i.e., a flat surface). However, from the various example embodiments shown in Launay, a required aspect thereof is that the antenna wirings 10, underlying the integrated circuit 1 in the cavity, be provided on a surface of the support (substrate) 2 which is recessed from the principle side thereof. It is also noted that, according to Launay's teachings, the board which includes the integrated circuit 1, the support substrate 2, the insulating strip layer 3 and the cavity 4 must have an upper surface that is defined by the upper surface of the strip layer 3. With regard to Figs. 20-21 thereof, further, such a relatively thick insulating strip layer is not employed. In fact, it is noted that none of the example showings in Launay show a mounting scheme on the principle surface of the support 2 of the semiconductor device in a manner as that called for in each of above-listed independent claims 1, 2, 26 and 30. Also, the wiring disposed on the substrate 2, in Launay, is the antenna wiring 10, which, it is observed, is embedded in a cavity in the support substrate 2 underlying the integrated circuit 1. Regarding Figs. 26 and 27 in Launay, also, it is noted that the integrated circuits 1 are not mounted on the principle surface of the support 2 but, rather, on the

recessed portion of a relatively thick insulating strip layer 3.

Launay disclosed an IC card structure in which a semiconductor device is mounted on the wiring substrate through a bump and, especially, where the electric connection terminal is disposed on a recessed portion of the substrate (e.g., support substrate 2), in clear contradistinction with that presently called for. Launay's scheme further features external connecting terminals that are, basically, contact shoes (i.e., external contact zones). The present invention, on the other hand, was implemented to be suitable for a semiconductor module employing bumps as external connection terminals for electrically mounting the module to an external board. If, therefore, a bump structure is employed with regard to Launay's construction, problems would arise. For example, the presence of bump electrodes would cause abrasion at the tips and, also, would lead to cracks at the root of the bumps. In other words, the teachings in Launay's disclosure limits the external connection terminals to flat external pads without bumps (i.e., without protruding conductors). Otherwise, Launay's construction would become defective.

The wiring substrate of the present invention, in clear contradistinction with the teachings of Launay, is such that the entire principle side thereof is represented by a common planar surface and has a coefficient of expansion which is closer to the coefficient of linear expansion of the semiconductor device. The present inventors have schemed the construction of a semiconductor module that utilizes a wiring substrate, which may be made of silicon, ceramic or glass, having a coefficient of expansion which is closer to the coefficient of linear expansion of the semiconductor chip(s) so as to effect a reliable flip-chip connection to the wiring substrate.

It is argued that the combined teachings of Launay and Yukawa, in effect, would have lead one of ordinary skill to consider the insulating strip layer 3 of Launay as a stress relaxing layer in a manner as that called for in each of the independent claims. It is submitted, however, such could not have been realized therefrom noting that the usage of the material, purpose, the way the respective insulating layers are applied, the operation associated therewith and the effects realized are completely different between that taught in Yukawa and Launay.

Yukawa, it is submitted, disclosed a resin-based thermo-plastic composite layer 12 which is composed of a lower thermo-plastic film bonding layer 12a and an upper paste-based bonding layer 12b, as in Fig. 1 thereof. That is, the layer 12 acts as a bonding layer between the radiator plate 10 and the chip 14 in Fig. 1. The technical idea in Yukawa regarding this is to assure adequate heat dissipation. On the other hand, Launay's scheme features an insulating strip 3 (formed of thermo-plastic material) that is provided between the antenna and the external connection terminals (external contact zones). (Column 1, lines 45-48, in Launay.) It is submitted, therefore, that the resin-based thermo-plastic material of Yukawa is not only implemented differently than the insulating strip 3 in Launay but, moreover, is used for a totally different purpose therefrom. Bonding is a characteristic whose purpose is to effect the joining of different parts such as between the rear surface of the chip 14 and the radiator plate 10 in Fig. 1 of Yukawa. With regard to Launay, the characteristics associated with the insulating strip layer 3 thereof concerns electrical isolation. It is apparent, therefore, applicants submit, both the strategic placement as well as operation and effects regarding the insulating strip layer 3 of Launay and the composite bonding layer 12 of Yukawa are completely different. It is submitted, therefore, in view of at

least the above differences therebetween, one of ordinary skill could not have envisioned electrical insulation characteristics from the bonding consideration associated with the composite layer 12 of Yukawa.

It is also noted that while the integrated circuit 1 of Launay's structure is disposed face-down inside the cavity (recessed portion), the semiconductor chip 14 in Fig. 1 of Yukawa is bonded via its rear surface to the radiator plate 10. For these and other reasons, one of ordinary skill, it is submitted, could not have been led to compose an insulating resin layer, as called for according to the respective independent claims and as further defined according to the corresponding dependent claims thereof, in view of the teachings of strictly using a resin-based composite layer as a bonding agent, according to Yukawa. Other than through the ability of hindsight reconstruction, the invention, it is submitted, could not have been rendered obvious in view of the combined teachings of Launay and Yukawa.

For at least the above reasons, the invention according to claims 1, 2, 5-8, 10-14, 24, 26, 27, 30 and 31 could not have been realizable from the combined teachings of Launay and Yukawa. As to the particularly featured aspects called for in claims 6 and 7, they are also unobvious over that same combination for at least the reasons given hereinabove. For example, dependent claim 6 further calls for the insulating resin layer to be "frame-shaped" such as shown in Figs. 1, 6, etc. in the present application. From Figs. 1 and 10 of Launay, however, the shape of the strip layer 3 is, clearly, not a frame-shape. Further, insofar as related to that set forth in dependent claim 7, the gradient of an outer circumferential side of the strip layer 3 from Fig. 10 of Launay, it is submitted, is not ascertainable. It is further alleged that it would have been obvious to "have a plurality of insulating resin layers instead of one insulating layer ... " as set forth in claim 8. However,

as discussed in the Specification in connection with Fig. 17 of the drawings, for example, one reason for dividing the insulating layer 3 into plural layer portions, is to provide ventilation for purposes of heat dissipation. In contradistinction with this, Launay neither disclosed nor even hinted at providing ventilation for purposes of heat dissipation. For the above reasons, the invention covered by the above listed claims could not have been rendered obvious from the combined teachings of Launay and Yukawa.

II. Rejection of claims 3 and 4 over the combination of Launay and Yukawa, *supra*, and further in view of Shoji (USP 6,242,932).

The supportive discussion in Part I above including the rebuttal arguments to the rejection based on Launay in view of Yukawa are to be considered as also being applicable herein.

It is admitted, in the rejection of claims 3 and 4 that, in effect, the combination of Launay and Yukawa did not teach forming the insulating layer by mask printing. From Shoji, however, it is alleged that " ... applying a resin layer or film by a mask printing process would yield printed pattern of the resin. " However, these references, even when considered combinedly, did not teach controlling the shape of the insulating resin layer in accordance with the printed circuit pattern scheme, an example of which is shown in connection with Figs. 10A-10B and 12 of the present application. It is submitted, therefore, for the same and similar reasons as that argued in connection with claims 1, 2, etc., and in view of the additional discussion herein, the invention according to claims 3 and 4 could not have been rendered obvious from the combined teachings of Launay-Yukawa in view of Shoji.

III. Rejection of Claim 9 over Launay-Yukawa and further in view of Hembree.

The supportive discussion and rebuttal arguments regarding independent claim 1 provided under Part I, above, are also applicable herein. Hembree was again strictly cited for its showing that a substrate such as interconnect substrate 56 (see Fig. 3B) can be a glass substrate. Hembree's structure, which is directed to an interposer for semiconductor devices, does not overcome the deficiencies, it is submitted, in Part I above regarding the combined teachings of Launay and Yukawa. In fact, Hembree neither suggested using glass or silicon material of a flat surface in a construction scheme as that presently called for in present base claim 1, which facilitates fine wiring formation including the interconnection between the semiconductor device and external circuitry to the module via the fine wiring. For at least the same reasons as that presented in Part I, above, as supplemented herein, the invention according to claim 9 also is considered patentable.

IV. Rejection of claims 15-19, 21 and 25 over the combination of Launay-Yukawa and further in view of Lee.

Since the claims in this rejection are also inclusive of the main featured aspects called for in claims 1+ such as discussed hereinabove, the above supportive discussion/rebuttal arguments regarding the applicability of Launay in view of Yukawa, are also applicable herein. As stated earlier in these remarks, the present invention calls for among the featured aspects thereof, a wiring substrate, which may be made of silicon, ceramic or glass, which has wiring disposed thereon and has a coefficient of expansion which is close to the

coefficient of linear expansion of the semiconductor device so as to safely support a flip-chip connection which can be reliably effected without using an underfill (see Figs. 29, 30, etc. of the present application). Lee also disclosed mounting a semiconductor device on a wiring substrate without using an underfill. However, with regard to the referred to Figs. 1A, 1C, 2 and 3 in Lee, there is no showing therein of a flip-chip connection that also does not require underfill, as that according to the present invention. Lee, it is submitted, simply disclosed a non flip-chip without use of underfill.

Regarding the invention set forth in the now independent claim 25, an example of which is shown with regard to Fig. 19 of the drawings in which the semiconductor device is die-attached to module 2 and is electrically connected to the wiring formed on the wiring substrate by wiring bonding. In accordance with this scheme, the heat dissipation is effected via the module substrate 2. As can be seen from Fig. 19 of the present application, although not limited thereto, consistent with that called for in claim 25, the entire principle side of the wiring substrate 2 on which the semiconductor device 15 is mounted on has a common planar surface and, moreover, the device is electrically connected to the wiring formed on the wiring substrate by wire bonding. For at least the above supportive discussion/rebuttal arguments against the rejection of claim 1 and as supplemented herein, the invention according to claim 25 could not have been rendered obvious.

V. Rejection of Claim 20 over the combined teachings of Launay-Yukawa and Lee and further in view of Shoji.

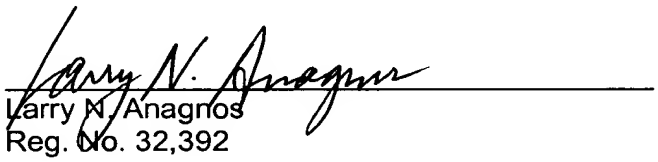
Launay-Yukawa and Lee and were applied as in the rejection of claims 1

and 16 and, moreover, Shoji was also applied similarly as that with regard to claims 3 and 4. Therefore, the same and similar reasons as that applied in favor of patentability of claims 1, 3-4 and 16, are also applicable herein.

Therefore, in view of the amendments presented hereinabove, together with these accompanying remarks, reconsideration and withdrawal of the outstanding rejections as well as favorable action on all of the presently pending claims and an early formal notification of allowability is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (500.40506X00), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



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